High-Speed Power System Transient Stability Simulation Using Highly Dedicated Hardware

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***Abstract*—This paper presents a fully analog demonstrator based on power system emulation for high-speed power system stability analysis. A benchmark using a fixed two-machine topology has been implemented. The characteristics of the emulated components (i.e., generators and transmission lines) are reprogrammable and short circuits can be emulated at different distances from the generator. This first realization is limited to transient stability analysis, as the main focus during design was put on computation speed. Indeed, the emulated phenomena are 10 000 times faster than real time. Moreover the authors aim to emphasize that such highly dedicated computation architectures are not only competitive in terms of speed, but also in terms of modularity.**

***Index Terms*—Analog emulation, analog integrated circuit, application specific integrated circuit (ASIC), power system simulation, power system stability.**

I. Introduction

A. Motivation

POWER system emulation, first introduced by [1], aims to accelerate power system dynamic simulation by using dedicated analog hardware. The idea is to avoid the heavy numerical matrix calculation of the grid. In this respect, we use an instantaneous analog Kirchhoff grid and we connect to the generator model equation solvers as well as the load model equation solvers (see Fig. 1).

A brief look at the history of power system stability simulation shows that analog simulation techniques are not a new invention. Indeed, before the emergence of numerical simulation methods in the 1960s, analog simulation methods were predominant [2]. Modern VLSI technologies can overcome the drawbacks which caused the disappearance of analog computation units [3]. Hence, in combination with the advances in CMOS technology, power system emulation delivers therefore improvements for three major concerns of nowadays power system simulators:

1) **Simulation time:** All the model solvers instantaneously discern the results of the others. It becomes possible to move faster than real time due to intrinsic parallelism of the computation as the simulation time becomes independent of topology size.
2) **Cost:** Custom fully integrated solutions are much cheaper than currently used high-performance numerical simulators (e.g., EUROSTAG, RTDS, etc.). Indeed, the cost of application specific integrated circuits (ASICs) is dependent on the area of silicon used and inversely dependent on the quantity of fabricated chips. For a quantity of 1 million ASICs containing each 100 power system nodes fabricated in a custom CMOS technology the price is reduced to a few dollars per chip.
3) **Size:** The dedicated hardware is much smaller than the bulky general use hardware and becomes therefore autonomous. Hence, such hardware could be integrated locally in power system components for control or screening actions.

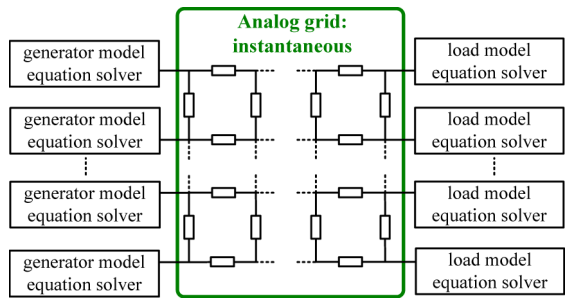

Fig. 1. Conceptional view of power grid emulation.

Analog emulators can therefore be seen as complements to numerical simulators with the advantage of speed, portability, low cost and autonomous functioning. One can imagine that analog emulators are used to detect critical situations by screening which can in the following lead to detailed analysis by numerical simulators.

B. State of the Art

Currently, three different implementations of power system dynamic simulation using analog emulation are under development. Their progress can be found in the literature [4]–[11]. These implementations are based on two different modeling approaches called "Phasor emulation approach" and "AC emulation approach", respectively.

The Phasor emulation approach [1], [4]–[7] is based on a mathematical representation of the grid. It uses a complex representation of voltages and currents in the grid. Two isolated and resistive networks are thus realized in order to emulate

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TABLE I
STATE OF THE ART OF THE DIFFERENT ANALOG EMULATION DEMONSTRATORS THAT APPEAR IN THE LITERATURE

	Approach	Description						Analysis	#buses, modularity	Speed up (computation time only)	Ref
		Generator		Grid		Load					
		Models	Implementation	Model	Implementation	Models	Implementation				
Fabre, Nagel et al.	Phasor emulation	Classical model	Analog, discrete electronics	Π-Model, *L* only	Analog, discrete components	Constant current model	Analog, discrete electronics	Transient stability	3, fixed topology	100x faster than real time	[4]
	Phasor emulation	Model reconfigurable (Classical, Park, etc.)	Numerical, microcontroller	Π-Model, *L* only	Analog, discrete components	Model reconfigurable	Numerical, microcontroller	Transient stability	16, modular topology	1000x faster than real time	[4,5]
Deese, et al.	Phasor emulation	Classical model	Analog, FPAA[2]	Π-Model, *L* only	Analog, FPAA[2]	Exponential recovery model	Analog, FPAA[2]	Transient stability	3, fixed topology	Real-time	[6,7]
Nagel, Fabre et al.	AC emulation	Classical model	Analog, dedicated partly integrated, partly discrete hardware	Π-Model, *R(fix), L(var), C(fix)*	Analog, dedicated integrated hardware	*RLC*-impedance	Analog, dedicated integrated hardware (not yet implemented)	Transient stability	2, fixed topology	10 000 times faster than real time	In this paper

[1] Field Programmable Gate Array (FPGA), [2] Field Programmable Analog Array (FPAA)

separately the real and imaginary part of the grid's current and voltages. It provides the downscaled envelopes of the real power system signals. The power grid is implemented with analog components, whereas the generator and load models can be implemented using purely analog, mixed or purely numerical implementations. AC emulation [8]–[11] is instead based on a one-to-one mapping of the components of the real power system by emulating their behavior on dedicated analog (micro)-electronics. Frequency dependence of the elements is preserved and the signals propagating on the emulated grid are the shrunk and downscaled current and voltage waves (AC signals) of the real power system. As such, this approach is termed AC emulation approach.

Several demonstrators have been realized for the different modeling approaches. Table I gives an overview of the state of the art.

C. Objective

This work is dedicated to AC emulation, the most recent power emulation approach. As an extension of the author's previous work, the first hardware demonstrator is presented. At this early stage of development, we focused on the speed aspect. Thus, the scope is to prove the high-speed capabilities of AC emulation with simple models, in fact, the models used at the beginning of power system simulation development. This permits to clearly separate microelectronic influences and power system theory aspects leading to precious conclusions for going a step further with less implementation risks.

This paper is divided into 7 sections: general approach to keep the modularity of analog emulators, general description of AC emulation emphasizing the differences between the two emulation approaches, specific description of the first AC demonstrator, behavioral model validation, microelectronic implementation with scaling issues, results of hardware testing and conclusion.

II. HOW TO GUARANTEE FLEXIBILITY?

One main consideration for simulators is their modularity. Analog emulation approaches are often seen as too rigid compared to numerical simulators. Indeed, in numerical simulators, the topologies, the characteristic of the elements and the models used to characterize the different power system components can

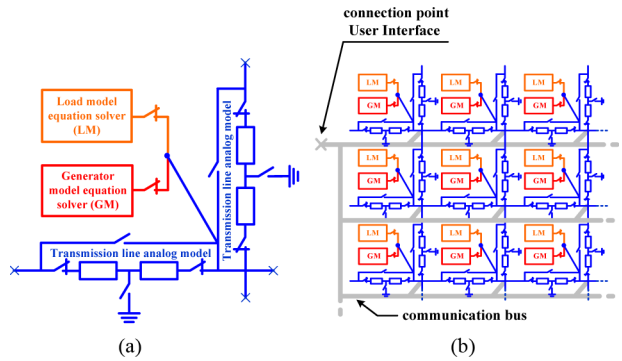

Fig. 2. a) PSA topology with analog interconnection points marked with a cross (x). b) Unprogrammed PSA array with schematized programming bus.

simply be changed through the software. No hardware changes are needed.

The authors developed a concept called Field Programmable Power Network System (FPPNS) [12] in order to enhance the flexibility of analog emulation approaches. The concept is based on an array of reconfigurable basic blocks called power system Atoms (PSA). Each PSA is composed of the basic elements of a power system. Hence it contains at least a generator model (GM), a load model (LM) and some analog transmission line models. The analog transmission lines are used to interconnect the atoms. Fig. 2(a) shows a possible PSA topology. Each element of a PSA is not only reprogrammable but is also equipped with switches. Therefore it is possible to emulate different power system topologies and scenarios without changing the hardware. A possible PSA array is depicted in Fig. 2(b). It includes PSA atoms connected through their transmission lines and a communication bus.

A user flow example is depicted in Fig. 3. The power system topology under investigation and the system parameters are set through the UI (i.e., a personal computer). This information is then converted into the corresponding emulated network parameters and transmitted to the PSA array through the communication bus.

Once the initial values are set, the operating point of the network (known as the steady state of the power system) is automatically reached and the system is ready to emulate the response of the power system to a particular perturbation. Rel-

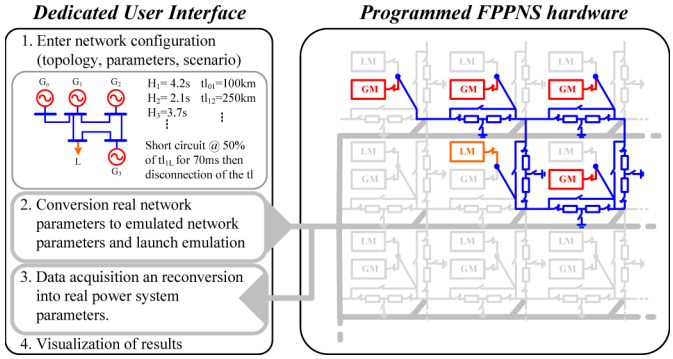

Fig. 3. Example of a programmed PSA array and its UI.

evant data is extracted and evaluated on-chip. Therefore, only a limited amount of information has to be sampled and transmitted to the UI for monitoring.

With such an approach, the flexibility of emulation becomes comparable to the flexibility of numerical simulators in terms of topology and configurability of the elements. The authors are aware of the fact that FPPNS does not guarantee the flexibility in terms of models. This flexibility depends entirely on the implementation of the generator and load models. Pure analog implementations are thus more rigid in terms of models than mixed-signal implementations such as proposed by Fabre *et al.* (see Table I) for Phasor emulation.

III. AC Emulation Approach—General Considerations

A. Concept

Phasor emulation provides the downscaled envelopes of the real power system signals. Frequency dependence of the elements is thus lost. AC emulation aims to keep frequency dependence of the elements. Theoretically, it becomes possible to simultaneously analyze various types of stabilities with different time constants after the occurrence of a contingency. Practically, of course, this depends additionally on the models that are implemented. A high-speed, multiple-phenomena-in-one simulator would be a very powerful tool for upcoming power system challenges which could be achieved using AC emulation.

B. Emulation Time

Due to grid emulation, the simulation time becomes independent of the topology size. Indeed the computation becomes intrinsically and massively parallel. Speed of AC emulation is consequently determined by frequency transposition. The emulated power system is working at a much higher frequency f_{tr} than the real power system f_{rps} (i.e., 50 Hz in Europe), thus ensuring that the emulated phenomena will be much faster than their real duration. The time scaling factor α connecting real and emulated time, can thus be defined as follows:

$$\alpha = \frac{f_{tr}}{f_{rps}}. \tag{1}$$

The higher the operating frequency f_{tr} in the emulated world, the shorter is the emulation time. f_{tr} is determined by the bandwidth of the emulated elements (specified in Section VI).

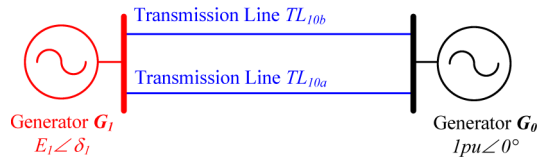

Fig. 4. Topology of the first AC emulator: single-machine infinite bus system.

This is an advantage compared to mixed-signal Phasor emulation implementations, where the emulation speed is limited by the speed of the analog to digital (AD) and digital to analog (DA) converters needed to pass from the analog domain to the numerical domain and vice versa.

C. Shrink and Downscaling

In addition to the time shrink, a downscaling also has to be introduced to map the real power system on the emulated microelectronics world. Therefore, the following parameters are defined: $\boldsymbol{k}_v$ (voltage scaling), $\boldsymbol{k}_i$ (current scaling), $\boldsymbol{k}_Z$ (impedance scaling), $\boldsymbol{k}_S$ (power scaling). These parameters represent the 1 pu values in the emulated world and are determined by the characteristics of microelectronic implementation (i.e., CMOS technology, microelectronic modeling, etc.).

D. Demonstrator

As stated in the objectives in Section I-C, we propose a first demonstrator to confirm the high-speed capabilities and feasibility of AC emulation. In its first instance, this prototype is dedicated to the study of transient stability supposing symmetrical three-phase operation of the power system. Hence, single-phase equivalent circuits are used. Moreover, it will be a fixed topology prototype with reconfigurable component characteristics, as is shown in Fig. 4—a single-machine infinite bus system containing two parallel transmission lines.

This topology allows emulating:

— Short circuits at different distances on transmission line TL_{10a}

— The disconnection of transmission line TL_{10a} and/or TL_{10b}

IV. Modeling

The behavioral models of the three main power system components (generator, load and transmission line) are shown in the following.

A. Generator Model

1) Basics: We have chosen the classical model for the generator [13]. As illustrated in Fig. 5, the generator can therefore be implemented as a voltage source $[e(t)$ with $E'\angle\delta]$ with a constant magnitude E' behind a reactance X'_d and a feedback loop controlling the behavior of the power angle δ according to the swing equation:

$$M\frac{d^2\delta}{dt^2} = P_m - P_e(\delta). \tag{2}$$

M is the inertia factor, P_m is the mechanical power, and P_e the active power provided to the power grid.

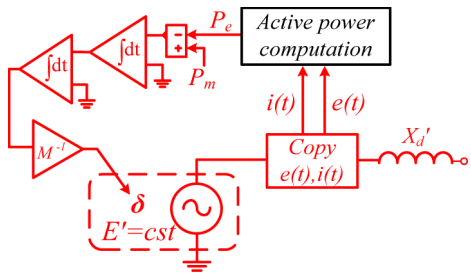

Fig. 5. Classical generator model adapted to AC emulation.

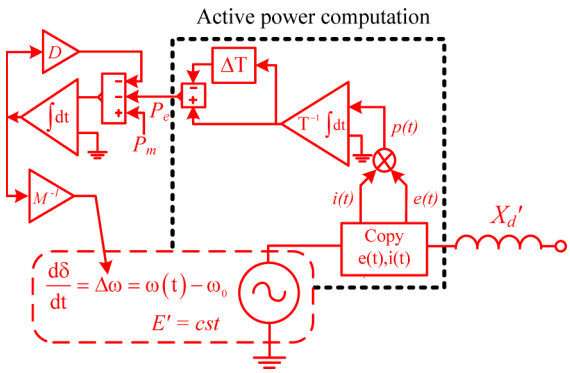

Fig. 6. Straightforward AC generator model.

The input of the feedback loop solving the swing equation (2) is the active power at the terminal of the generator. Because the signals propagating in the emulated grid of the AC emulation approach are the shrunk and downscaled current and voltage waves of the real power network and because of the fact that we are using single-phase equivalent circuits, we have only direct access to the instantaneous current [$i(t)$ with $I\angle\phi$] and voltage [$e(t)$ with $E'\angle\delta$] sine waves at the terminal of the generator. A block to compute the active power has to be added. This additional unit has no physical meaning. Its impact has to be carefully evaluated.

2) Straightforward Implementation: Multiplying $i(t)$ and $e(t)$ makes the instantaneous power $p(t)$ available quasi instantaneously. The relationship between $p(t)$ and the active power P_e is as follows:

$$P_e = \frac{1}{T}\int_{t-T}^{t} p(t)\,dt \tag{3}$$

with T, the period of the current and voltage sine wave, respectively. Therefore the system level of the straightforward model of the generator becomes as depicted in Fig. 6.

The ΔT-block delays the signal at its input by T. Note that the signal at the input of the sine wave generating unit is not $\delta(t)$ but $\Delta\omega$ because this block will be implemented using a voltage controlled oscillator (VCO) and the link between the angle $\delta(t)$ and the angular frequency $\omega_{osc}(t)$ of the VCO output signal is defined as

$$\omega_{osc}(t) = \omega_0 t + \underbrace{\int_0^t \omega(t)dt}_{\delta(t)}. \tag{4}$$

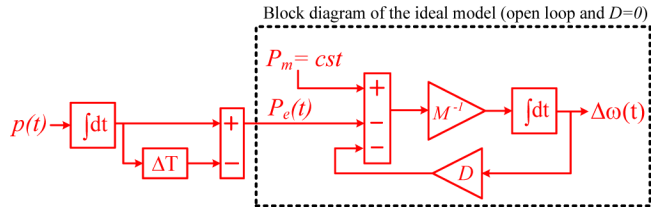

Fig. 7. Ideal and straightforward emulated swing equation computation.

Thus, the step from $\Delta\omega$ to $\delta(t)$ is not necessary in the feedback loop as this operation is intrinsic to the sine wave generating unit.

Behavioral simulations are presented in [10] and [11] and have shown that the active power computation block introduces an error. This error can be considerably reduced by adding damping in the feedback loop.

The analysis of this model shows that instead of solving (2), the following equation is solved by the emulated generator:

$$M\frac{d^2\delta}{dt^2} = P_m - \underbrace{\frac{1}{T}\int_{t-T}^{t} p(t)dt}_{=P_e} - P_D(\dot{\delta}). \tag{5}$$

Two supplementary elements appear:

— The factor P_D represents the damping power. It is proportional to $\Delta\omega$ according to the following equation:

$$P_D = D\frac{d\delta}{dt} = D\Delta\omega. \tag{6}$$

D is called the damping coefficient.

The term P_D has been added to damp the oscillations for finding as fast as possible the steady state of the system after initialization of all parameters. During the emulation of a given scenario, D is ideally set to zero, thereby not influencing the emulation result.

— The supplementary integration needed to extract P_e introduces most notably a delay of at least one period in the feedback loop. The corresponding part is highlighted in Fig. 6. This delay does not reflect reality and consequently has to be considered as a systematic error.

In order to quantify this error, an open-loop characterization of both swing equation computation models, the ideal and the emulated ones (both depicted in Fig. 7), was performed.

In this process, the non-linear sine wave generating unit was omitted, as it is the same in the two loops. Moreover, for simplifying analytical calculations, the output was quantified in the Laplace domain and only the final result was then retranslated back to the time domain.

The output function of the ideal model ($D = 0$) is as follows:

$$\Delta\omega(t) = \frac{1}{M}\int_0^t (P_m - P_e(t))dt. \tag{7}$$

Thus, ideally, the temporal weighting is uniform. In the emulated model, again with $D = 0$, the present has no influence on the result. An integral effect appears:

$$\Delta\omega(t) = \frac{1}{M}\int_0^t (P_m - (p(t-\tau) - p(t-\tau-T))\tau)d\tau. \tag{8}$$

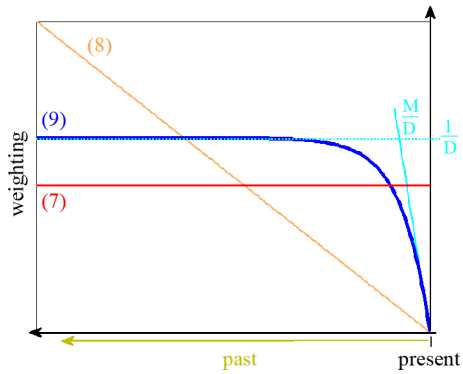

Fig. 8. Weighting as calculated in (7), (8), and (9), respectively.

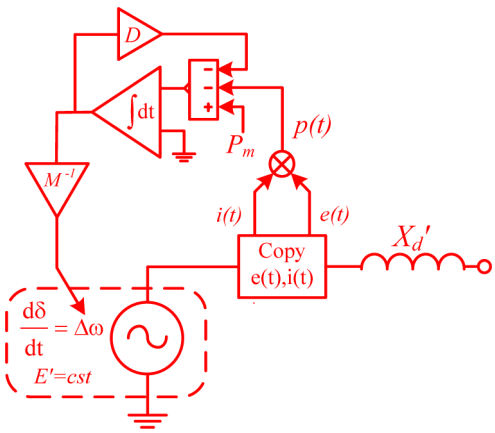

Fig. 9. Optimized AC generator model.

Finally the output function of the emulated model when the damping is added $D \neq 0$:

$$\Delta\omega(t) = P_{\mathrm{m}}\frac{1-e^{-\frac{D}{M}t}}{D} - \int_0^t \left((p(t-\tau)-p(t-\tau-T))\frac{1-e^{-\frac{D}{M}t}}{D}\right) d\tau. \quad (9)$$

As opposed to the previous case, the weighting tends here towards a constant value. Fig. 8 illustrates these behaviors.

This analysis proves that keeping a damping factor after the fault considerably reduces the systematic error introduced by the active power computation block. An optimal value (i.e., where the systematic error is minimal) for D exists. Nevertheless, with these formulas only an approximate optimal numerical value is obtained, because in reality all generators are interconnected, thus sharing their errors mutually. Only a qualitative minimization of the systematic error is thus possible. Another bottleneck of this solution is the possible instability of the feedback loop caused by the two integrators. A considerable design effort would be needed to guarantee stability.

3) Optimized Implementation: An optimized model omitting the supplementary integration introduced by the computation of the active power is presented in Fig. 9. Thereby, we directly use the instantaneous power $p(t)$ instead of the active power P_e. Consequently, the equation that is solved by the emulated generator is

$$M\frac{d^2\delta}{dt^2} = P_m - p(t) - P_D(\dot{\delta}) \quad (10)$$

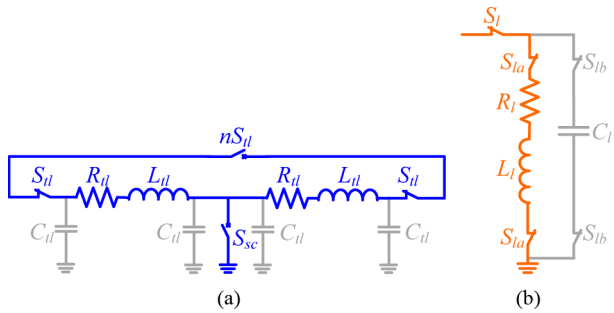

Fig. 10. a) Transmission line model. b) Load model.

with all the parameters as defined before. Moreover, this solution is certainly stable on the system level because there is only one integrator; hence, the maximum phase shift at unity gain is $-\frac{\pi}{2}$.

Supposing $P_D = 0$, and $p(t) = u(t)\ i(t)$ then (10) becomes

$$M\frac{d\omega(t)}{dt} = \mathrm{P}_m - \underbrace{E'I\cos(\delta-\phi)}_{=P_e} - \underbrace{E'I\cos(2\omega\, t+\delta+\phi)}_{systematic\ error\ e}. \quad (11)$$

Obviously, a systematic error exists here as well. In order to be coherent, we also express the influence of this error on the output function $\Delta\omega$ (as done for the straightforward implementation). In this scope, we integrate the systematic error e found in (11), obtaining

$$e_{\Delta\omega} = \frac{E'I}{2M\omega}\left(\underbrace{\sin(\delta+\phi)}_{constant} - \underbrace{\sin(2\omega t+\delta+\phi)}_{oscillating}\right). \quad (12)$$

As they are divided by $\frac{1}{2\omega}$, both the amplitude of the oscillating part of the error as well as the frequency-independent part of the error are negligible compared to the useful signal $\Delta\omega$.

B. Transmission Line Model

The emulated transmission line model is based on the well-known pi-equivalent model for transmission lines with its entire elements reprogrammable. This equivalent circuit is valid for much shorter lines than the wavelength so that the line parameters can be assumed to be uniformly distributed over the whole line length [13]. In order to be able to create short circuits at different distances from a node, two of these pi-models are connected in series with a switch S_{sc} to ground in their middle. Fig. 10(a) shows this configuration. The switches S_{tl} are, on the one hand, needed to configure the topology together with switch nS_{tl} and, on the other hand, to emulate line disconnections.

C. Load Model

A load is characterized by its active and reactive power. For modeling this, a resistance and inductance in series are sufficient. In order to compensate, reactive power capacitors are connected to power system nodes. Hence a capacitance is included in the load model [see Fig. 10(b)]. All elements need to be reprogrammable. The switches allow the load to be configured as follows:

— As RL. R characterizes the active power part and L the reactive power part.

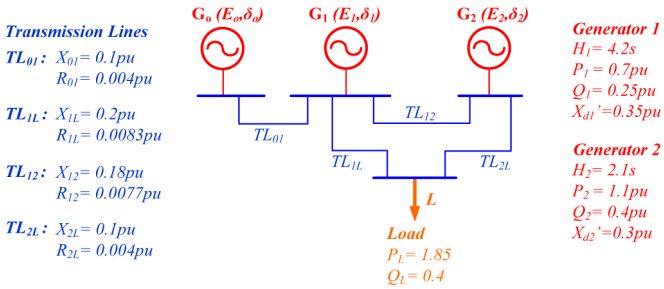

Fig. 11. Reference topology.

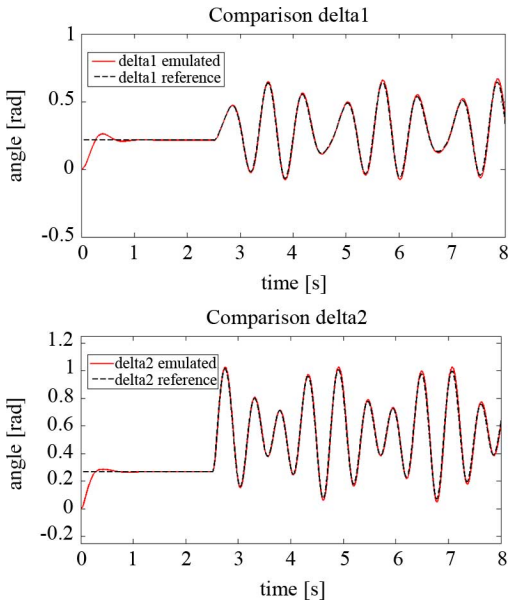

Fig. 12. Validation of the developed AC emulation component models.

TABLE II
ABSOLUTE ERROR WITHIN 1 S AFTER THE FAULT

Emulator		*D* [-]	Δ_{min} [°]	Δ_{max} [°]
Behavioral emulator	δ_1	0	-0.49	0.75
	δ_2	0	-1.18	0.95

TABLE III
COMPARISON OF CRITICAL SHORT-CIRCUIT TIME t_{crit}

Simulator / Emulator	*D* [-]	t_{crit} [ms]	Δ [ms]
Numerical reference simulator	0	181	---
Behavioral emulator	0	184	+3

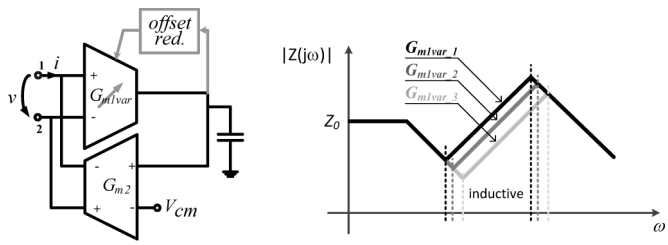

Fig. 13. Active inductor and its frequency behavior for different G_{m1var}.

TABLE IV
SHRINK AND DOWNSCALING PARAMETERS

	pu	*Real world*	*Emulated world*	
Voltage	1	380kV	k_v	80mV
Current	1	263A	k_i	4µA
Impedance	1	1444Ω	$k_v/k_i=k_Z$	20kΩ
Power	1	100MVA	$k_v\,k_i=k_S$	320nVA
Frequency	---	50Hz	f_{tr}	500kHz

— As $RL//C$. Active and reactive power parts are depending on the values of R, L and C. Capacitive, resistive and inductive effects can be emulated and there is an additional degree of freedom as compared to the simple RL-series-load.
— As C. Then the load is used to compensate the reactive power in the system.

The switch S_l is used to configure the topology and to emulate load disconnections.

V. BEHAVIORAL MODEL VALIDATION

1) Description of the Simulation Method: Behavioral simulations of the AC emulation models are performed in the Cadence IC-Virtuoso environment. The simulator used is Spectre [14]. This allows simulating power system topologies with the electronic AC models of the transmission lines and the load (as shown in Fig. 10) in combination with a purely behavioral AC generator model (as shown in Fig. 9). The obtained results are compared to the results of a numerical reference simulator implemented in LabView. This reference simulator has been validated by comparison to EUROSTAG as shown in [5].

2) Results: The 4-bus reference topology and the real-world characteristics of its elements used to validate the developed models are depicted in Fig. 11.

The reference scenario selected for comparison is as follows: 2.505 s after setting off the emulator, a short circuit is applied on the middle of the line between Generator G_2 and Load L. A certain time t_{sc} later, the whole line is disconnected. Note that the times and the results are converted into real world values. Hence, the speed enhancement of the emulator is not visible in this result comparison. In order to force a fast convergence of the system to the steady state values of δ_1 and δ_2, the damping factors D_1, D_2 of both generators are set at a high value at the beginning of the behavioral emulation. Then, at the moment of the short circuit, their values are set to 0.

Fig. 12 shows the comparison of the behavioral simulation results (called behavioral emulation results) and the results of numerical reference simulation while applying a short circuit t_{sc} of 70 ms in the scenario described above. Table II shows the absolute error of the emulations compared to the reference simulator within 1 s after the fault.

The main function of a transient stability power system simulator is to determine the critical short-circuit clearing time t_{crit}. Table III compares the emulated result for t_{crit} of the line between G_2 and L to the numerical simulation result.

As the validity of the chosen Classical generator model is limited, the information about stability is contained in the first oscillation after the fault. The developed models can therefore be validated through the presented results. These results confirm therefore, that the systematic error introduced by the AC generator model is negligible.

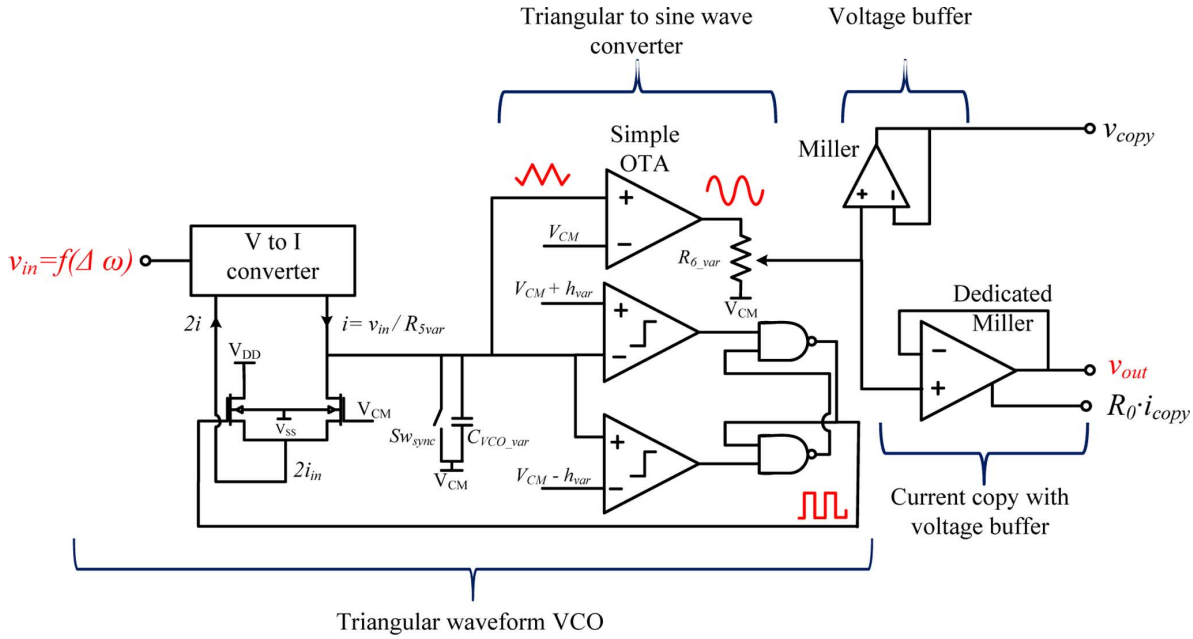

Fig. 14. Transistor level of the VCO including current and voltage copy used as input of the swing equation solver.

VI. Microelectronic Implementation

Table IV gives an overview of the optimal downscaling and shrink factors for the first AC emulator. These parameters are determined by two main issues. On the one hand, there is the chosen microelectronic technology: in our case the emulation is realized in a CMOS $0.35\ \mu\mathrm{m}$ technology with 3.3 V supply voltage.

On the other hand, the parameters depend also on the designed microelectronic implementations of the components. Their linearity, noise and bandwidth characteristic are limiting factors. Therefore, the design of the inductance was particularly crucial. As further explained in the next section, the operating frequency of the first demonstrator is set to 500 kHz. Phenomena are therefore **10 000 times faster** than in the real world ($\alpha = 10\,000$).

A. Focus on the Inductance Implementation

Generator, load and transmission line model contain a reprogrammable inductance. Therefore, the inductance design becomes a key element for AC emulation. Considering shrink and downscaling factors as well as appropriate tuning ranges for all components, the designed inductance needs to be able to take values from 0.15 mH to 2.55 mH.

Passive integrated inductance topologies are not suited for this application as they are not tunable and as they occupy too much area. Moreover, known active inductance topologies [15] are not suitable for this application for two main reasons. First, most active inductors are used at very high frequencies as a result of their RF applications. Second, their DC characteristics lead to a saturation problem due to offset currents that occur when connecting them in a power system configuration. Hence, a custom, fully integrated and reconfigurable inductance had to be designed for power system AC emulation. As such, imperfection, calibration, mismatch and process variation aspects have been taken into account. Its topology is schematized in Fig. 13.

The inductance created with this topology is defined as

$$L_{\mathrm{var}} = \frac{C_{\mathrm{convert}}}{G_{\mathrm{m1var}} G_{\mathrm{m2}}} \tag{13}$$

and can be tuned by changing the transconductance G_{m1var}. The operating range of the inductor is limited. The limits set the optimal operating frequency of the prototype to 500 kHz. More details about the design can be found in [9] and the transistor-level design is presented in [16].

B. Focus on the Generator Implementation

The behavioral optimized generator model presented in Fig. 7 is realized with a pseudo-sine wave voltage controlled oscillator (VCO) as it is shown in Fig. 14. The VCO generates a triangular signal with linear relation between the input voltage v_{in} and the frequency f_{out} of the generated output signal:

$$f_{\mathrm{out}} = \frac{v_{in}}{4 R_{5var}\, C_{VCO}\, h_{var}}. \tag{14}$$

All parameters are defined in Fig. 14.

The triangular signal is then transformed to a pseudo sine wave using large signal characteristics of a differential pair. The error introduced by this distorted sine wave on emulation results is negligible [10].

In order to reduce the realization time, the swing equation solver of the generator is realized on a printed circuit board (PCB) with discrete electronics. Details are visible in Fig. 15 The internal inductance of generator G_1, X'_{d1} is contained in L_{1avar} and/or L_{1bvar}.

Consequently, the implemented swing equation can be expressed as follows:

$$\underbrace{v_{in}}_{d\omega/dt} = \underbrace{\frac{G_2}{R_{1var}C} v_{P_m}}_{\frac{1\alpha^2}{Mk_S} P_m} - \underbrace{\frac{R_0 G_1}{R_{2var}C} e(t) i(t)}_{\frac{1\alpha^2}{Mk_S} p(t)} - \underbrace{\frac{k}{R_{3var}C} \int v_{in}}_{\frac{1\alpha^2}{Mk_S} P_D} \tag{15}$$

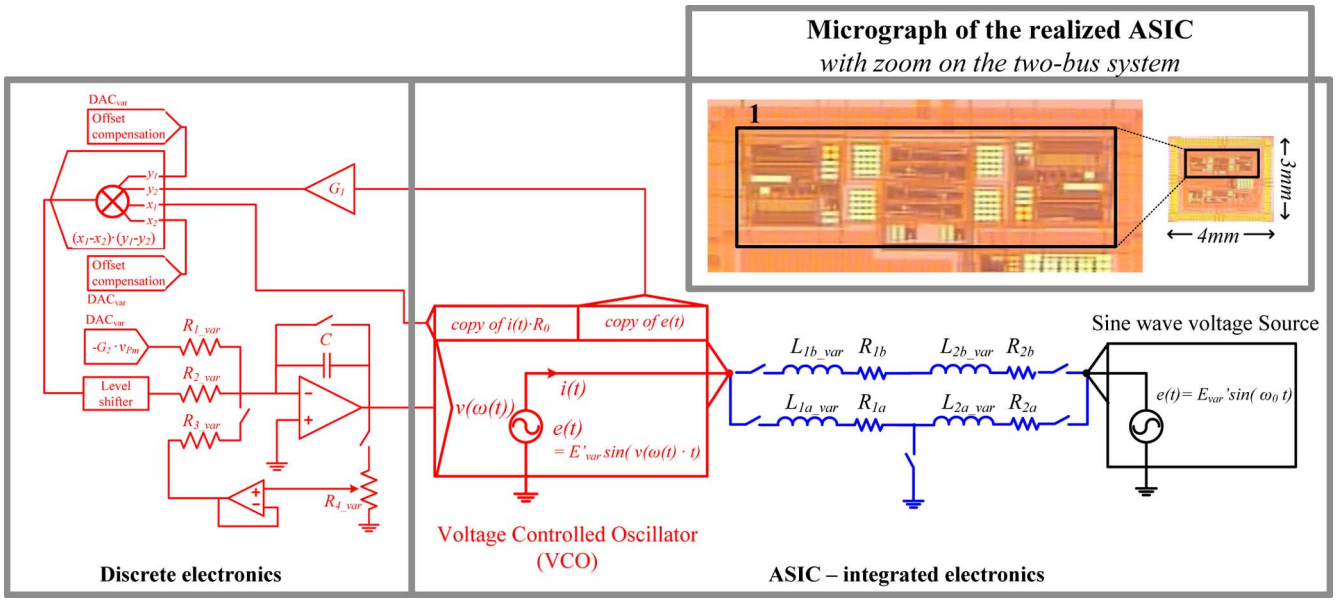

Fig. 15. Detailed system level of the first demonstrator and micrograph of the realized ASIC with zoom on the two-bus system.

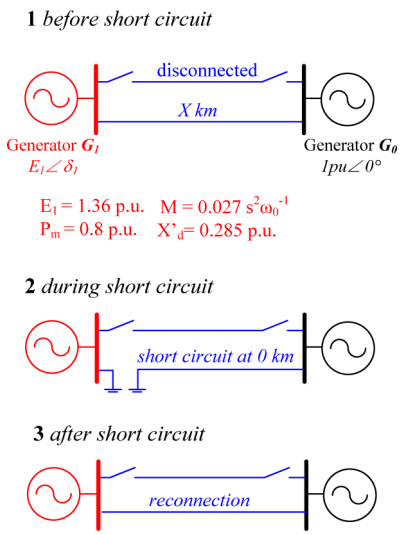

Fig. 16. Emulated scenario.

where k is the attenuation factor set by the potentiometer R_{4var}.

Comparing (15) to (10) and considering shrink and downscale factors of Table IV, the parameters have to be set to fulfill the following equation:

$$\underbrace{\frac{G_2}{R_{1var}C} = \frac{R_0 G_1}{R_{2var}C} = \frac{1}{M}\frac{\alpha^2}{k_S}}_{corresponding\ to\ 1/M\ in\ the\ real\ world} . \qquad (16)$$

All parameters are defined in Fig. 16 and Sections III-B and III-C.

The components containing the suffix *var* are programmable through Serial to Parallel Interface (SPI). The infinite bus (Generator G_0) is implemented using the same VCO as seen in Fig. 14. Contrary to generator G_1 the input voltage of v_{in} is set to a constant value in order to keep its frequency constant.

VII. ASIC Measurement Results

A. ASIC

A micrograph of the realized ASIC is shown in Fig. 15. Block 1 contains the single-machine infinite bus system with SPI control units and the biasing of the VCO. The maximum power consumption at steady state is 10.2 mA and the area occupied by the two node system is $1.35\ \mathrm{mm}^2$. A single inductance containing 61 transistors occupies an area of $0.15\ \mathrm{mm}^2$ and a VCO $0.35\ \mathrm{mm}^2$.

The other blocks visible on the ASIC are for testing and characterizing the developed components separately.

B. Measurement Results

The implemented scenario is shown in Fig. 16. The operating frequency was set to 500 kHz. Figs. 17 and 18 illustrate the first measurement results of the real emulator. Calibration was done manually.

The AC emulation demonstrator, which is composed of the designed microelectronic elements and the reduced swing equation block, which is implemented by discrete components on the PCB, works accurately. Results are obtained 10 000 times faster than real time, confirming the high-speed capabilities of AC emulation (**1 μs** in the emulated world corresponds to **10 ms** in the real world). Fig. 17 affirms that reproducible and accurate results are obtained for steady-state evaluations of different topologies.

Nevertheless, the reader could question the robustness of AC emulation. Indeed, contrary to the steady-state evaluations, repeatability of critical clearing time (CCT) results is limited and leads to a range of results, as illustrated in Fig. 18. This can be traced back to the two imperfections, which appear after the fault:

1) The saturation of the current during the short circuit.
2) An inadvertent damping after the fault

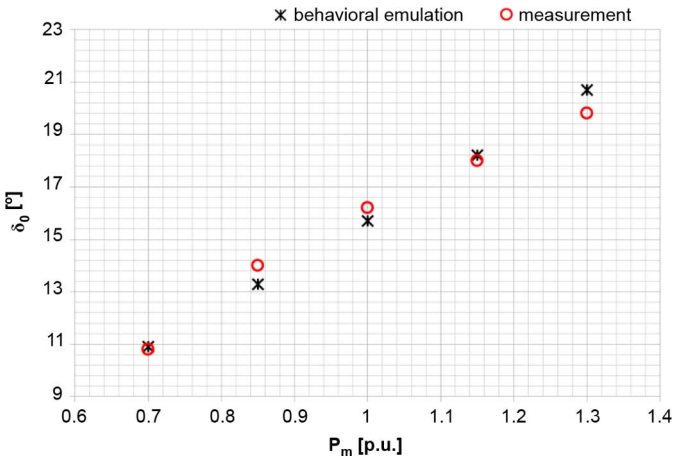

Fig. 17. Electrical angle of Generator G_1 at steady state δ_{1_0} for different P_m-values and repetitive measures.

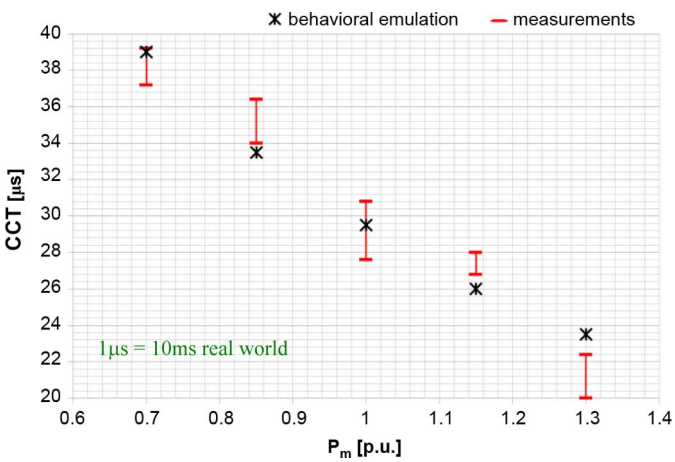

Fig. 18. CCT measurement results for repetitive measures with a resolution of 700 ns and changing P_m-values.

The saturation leads to an error in the instantaneous power computation only during the short circuit and falsifies consequently slightly the CCT results. The underestimation of the current needed during a short circuit is at the origin of this imperfection. Providing more current in the output stages during the redesign of the analog building blocks solves this problem entirely.

Different sources or a combination of them lead to the second imperfection. First, the saturation of the current during the short circuit can assist to the appearance of a damping as late effect. Transistor-level simulations confirm, however, that it cannot be the unique source of this damping. Second, the CM-variation of the current can cause this damping due to the fact that it causes saturation of the externally added multiplier. This can be identified as the starting point of the damping.

As the damping starts to appear only at the edge of the first oscillation after the fault, it has only marginal impact on the CCT results. That is why the emulation results remain within an acceptable range of $\pm 15\%$ of the simulated values. This permits to validate the functionality of the demonstrator. A dedicated microelectronic implementation of the external feedback loop, taking into account the possible CM-variations during the design of the dedicated multiplier, will remove the damping. Moreover the CM-variations at the input of the multiplier will be decreased because the signals can be kept smaller in the case of an integrated solution.

In sum, the promising speed capabilities and the feasibility of AC emulation are largely confirmed. Moreover, it is important to note that only fully integrated solutions providing automated calibration utilities can guarantee robust and accurate results.

VIII. Conclusion

Power system emulators aim to complete nowadays high-performance and high-precision numerical simulators by proposing solutions to their speed, cost and size bottlenecks. Such high-speed emulators would certainly contribute to the operation security of the emerging Smart Grids.

This paper presents the successful achievement of the first step in the development of a large-scale, multi-phenomena, high-speed power system simulator based on AC emulation. Indeed, the first demonstrator is presented and confirms the high-speed capabilities (10 000 times faster than real-world phenomena) and the feasibility of such highly dedicated analog computation hardware. Moreover, the here presented work has shown that the AC emulation approach is ready to be implemented as FPPNS to go a step further and prove the suitability of such simulator for large-scale topologies. In parallel the development of more advanced power system component models should start.

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